

WE CLAIM:

1. A power supply with integral control circuit comprising:
a low voltage section for providing a control signal;
a high voltage section having an output for powering a load; and
a bridge section capacitively coupling the low voltage section to the high voltage section, the bridge section adapted to operate the high voltage section in response to a signal from the low voltage section.
2. A power supply according to claim 1 wherein the bridge section comprises an integrated circuit.
3. A power supply according to claim 1 wherein the bridge section comprises an integrated circuit and an external isolation capacitor.
4. A power supply according to claim 1 wherein the low voltage section further comprises an isolation capacitor.
5. A power supply according to claim 1 wherein the bridge section further comprises a first half wave rectifier and a second half wave rectifier.
6. A power supply according to claim 5 wherein the first half wave rectifier has a rise time faster than about 20 volts per microsecond.
7. A power supply according to claim 5 wherein the second half wave rectifier has a fall time faster than about 50 volts per microsecond.
8. A power supply according to claim 1 further comprising a first transistor having its base and emitter terminals coupled with the high voltage section for supplying power to the load, and its gate operably coupled to the bridge section.
9. A power supply according to claim 8 wherein the bridge section further comprises:
an isolation capacitor having one terminal coupled to the low voltage section output;
a forward-biased diode and first and second reverse-biased diodes coupled to the opposing terminal of the isolation capacitor;

a resistor and capacitor (RC) pair coupled in parallel with the forward-biased diode and the first reverse-biased diode; and

an NMOSFET having its gate terminal coupled with the RC and first reverse-biased diode, and its source terminal coupled with the RC pair, forward-biased diode and gate of the first transistor, and its drain terminal coupled with the second reverse-biased diode and base of the first transistor.

10. The power supply of claim 9 adapted for use with a low voltage section output within a frequency range of approximately 1 MHz-10MHZ.

11. The power supply of claim 9 wherein the RC pair exhibits a time constant within a range of approximately three to ten times longer than the minimum frequency used for the low voltage section output.

12. The power supply of claim 9 wherein the diodes comprise N+ substrate P- well bipolar transistors.

13. A full bridge rectifier driver circuit comprising:

a low voltage section for providing a high frequency control signal;

a high voltage section having an output for powering a load;

a bridge section capacitively coupling the low voltage section to the high voltage section, the bridge section further comprising a high portion adapted to operate the high voltage section in response to a high signal from the low voltage section and a low portion adapted to operate the high voltage section in response to a low signal from the low voltage section.

14. A full bridge rectifier driver circuit according to claim 13 wherein the bridge section comprises an integrated circuit.

15. A full bridge rectifier driver circuit according to claim 13 wherein the bridge section high portion and bridge section low portion comprise a first and a second integrated circuit.

16. A full bridge rectifier driver circuit according to claim 13 wherein the bridge section comprises an integrated circuit and an external isolation capacitor.

17. A full bridge rectifier driver circuit according to claim 13 wherein the low voltage section further comprises an isolation capacitor.

18. A full bridge rectifier driver circuit according to claim 13 further comprising:

a first transistor having its base and emitter terminals coupled with the high voltage section for supplying power to the load, and its gate operably coupled to the high portion of the bridge section; and

a second transistor having its base and emitter terminals coupled with the high voltage section for supplying power to the load, and its gate operably coupled to the low portion of the bridge section.

19. A full bridge rectifier driver circuit according to claim 18 wherein the bridge section high portion and low portion each further comprise:

an isolation capacitor having one terminal coupled to the low voltage section output;

a forward-biased diode and first and second reverse-biased diodes coupled to the opposing terminal of the isolation capacitor;

a resistor and capacitor (RC) pair coupled in parallel with the forward-biased diode and the first reverse-biased diode; and

an NMOSFET having its gate terminal coupled with the RC and first reverse-biased diode, and its source terminal coupled with the RC pair, forward-biased diode and gate of the first transistor, and its drain terminal coupled with the second reverse-biased diode and base of the first transistor.

20. The full bridge rectifier driver circuit of claim 19 adapted for use with a low voltage section output within a frequency range of approximately 1 MHz-10MHZ.

21. The full bridge rectifier driver circuit of claim 19 wherein the RC pair is selected to exhibit a time constant within a range of approximately three to ten times longer than the minimum frequency used for the low voltage section output.
22. The full bridge rectifier driver circuit of claim 18 wherein the diodes comprise N+ substrate P- well bipolar transistors.
23. An implantable cardiac defibrillator circuit comprising:
 - a low voltage section for providing a control signal;
 - a high voltage section having an output for powering a load; and
 - a bridge section capacitively coupling the low voltage section to the high voltage section, the bridge section adapted to operate the high voltage section in response to a signal from the low voltage section.
24. An implantable cardiac defibrillator circuit according to claim 23 wherein the bridge section further comprises a high portion adapted to operate the high voltage section in response to a high signal from the low voltage section and a low portion adapted to operate the high voltage section in response to a low signal from the low voltage section.
25. An implantable cardiac defibrillator circuit according to claim 23 wherein the bridge section comprises an integrated circuit.
26. An implantable cardiac defibrillator circuit according to claim 24 wherein the bridge section high portion and bridge section low portion comprise a first and a second integrated circuit.
27. An implantable cardiac defibrillator circuit according to claim 23 wherein the bridge section comprises an integrated circuit and an external isolation capacitor.
28. An implantable cardiac defibrillator circuit according to claim 23 wherein the low voltage section further comprises at least one isolation capacitor.
29. An implantable cardiac defibrillator circuit according to claim 24 further comprising:

a first transistor having its base and emitter terminals coupled with the high voltage section for supplying power to the load, and its gate operably coupled to the high portion of the bridge section; and

a second transistor having its base and emitter terminals coupled with the high voltage section for supplying power to the load, and its gate operably coupled to the low portion of the bridge section.

30. An implantable cardiac defibrillator circuit according to claim 29 wherein the bridge section high portion and low portion each further comprise:

an isolation capacitor having one terminal coupled to the low voltage portion output;

a forward-biased diode and first and second reverse-biased diodes coupled to the opposing terminal of the isolation capacitor;

a resistor and capacitor (RC) pair coupled in parallel with the forward-biased diode and the first reverse-biased diode; and

an NMOSFET having its gate terminal coupled with the RC and first reverse-biased diode, and its source terminal coupled with the RC pair, forward-biased diode and gate of the first transistor, and its drain terminal coupled with the second reverse-biased diode and base of the first transistor.

31. The implantable cardiac defibrillator circuit of claim 23 adapted for use with a low voltage section output within a frequency range of approximately 1 MHz-10MHz5.

32. The implantable cardiac defibrillator circuit of claim 23 wherein the RC pair is selected to exhibit a time constant within a range of approximately three to ten times longer than the minimum frequency used for the low voltage portion output.

33. The implantable cardiac defibrillator circuit of claim 23 wherein the diodes comprise N+ substrate P- well bipolar transistors.